EEE3050 Theory on Computer Architectures (Spring 2017)
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Appendix - Modules

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Part B: hazard module

- This module produces,
  - Forwarding control signals
    - **ForwardAD**
    - **ForwardBD**
    - **ForwardAE**
    - **ForwardBE**
  - **Stall** signal
    - To freeze IF and ID stage and flush the ID/EX pipeline register
      - Due to data hazard
  - **Flush** signal
    - To flush the IF/ID pipeline register
      - Due to control hazard (context switching)

Part C: branch_predictor module

- This module produces,
  - Branch Prediction signal: IF_prdTaken
  - Branch target address: IF_pc_bp

- This module stores,
  - Branching result: WB_btaken
  - Branched address: WB_btgt

Part C: misprediction_control module

- This module detects,
  - Branch misprediction
    - IF stage prediction vs. ID stage calculation
      - Taken or not
      - Address to go

- When detects misprediction
  - Stall the pipeline
  - Correct the program counter

The Big Picture