Midterm Exam Results
(Max = 190, Average = 85.55/200)
MIPS Pipeline

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MIPS Pipelined Datapath

Right-to-left flow leads to hazards
Pipeline Registers

- Need registers between stages
  - To hold information produced in previous cycle
Pipeline Operation

- **Cycle-by-cycle flow of instructions through the pipelined datapath**
  - “Single-clock-cycle” pipeline diagram
    - Shows pipeline usage in a single cycle
    - Highlight resources used
  - cf. “multi-clock-cycle” diagram
    - Graph of operation over time

- We’ll look at “single-clock-cycle” diagrams for load & store
IF for Load
ID for Load
EX for Load
MEM for Load
WB for Load

Wrong register number
Correct Datapath for Load
IF for Store
ID for Store

[Diagram of computer architecture]
EX for Store
MEM for Store
WB for Store

[Diagram of the WB for Store, showing the flow of instructions and data through the pipeline stages: IF/ID, ID/EX, EX/MEM, MEM/WD.]
Multi-Cycle Pipeline Diag. (1)

- Form showing resource usage
Traditional form

Program execution order (in instructions):

lw $10, 20($1)
sub $11, $2, $3
add $12, $3, $4
lw $13, 24($1)
add $14, $5, $6
State of pipeline in a given cycle

- add $14, $5, $6
- lw $13, 24 ($1)
- add $12, $3, $4
- sub $11, $2, $3
- lw $10, 20($1)
Pipelined Control (Simplified)

[Diagram of pipelined control system]

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Control signals derived from instruction
• As in single-cycle implementation
Pipelined Control (2)