Input/Output

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I/O Devices

- Usually includes some non-digital component
- Typical digital interface to CPU:
8251 UART

- Universal asynchronous receiver/transmitter (UART)
- Provides serial communication
- 8251 functions are integrated into standard PC interface chip
- Allows many communication parameters to be programmed
Serial Communication

- Characters are transmitted separately:

```plaintext
no char

start bit 0 bit 1 ... bit n-1 stop

time
```
Serial Comm. Parameters

- **Baud (bit) rate**
  - 50, 300, 1200, 2400, 4800, 9600, 14400, 19200, 38400, 57600, 115200 bps

- **Number of bits per character**
  - 5, 6, 7, 8 bits

- **Parity/no parity**

- **Even/odd parity**

- **Length of stop bit**
  - 1, 1.5, 2 bits
8251 CPU Interface

CPU

8251

status (8 bit)
data (8 bit)
xmit/rcv

serial port
Programming I/O

- Two types of instructions can support I/O:
  - Special-purpose I/O instructions
  - Memory-mapped load/store instructions

- Intel x86 provides in, out instructions. Most other CPUs use memory-mapped I/O

- I/O instructions do not preclude memory-mapped I/O
ARM Memory-Mapped I/O

- Define location for device (mem address)
  
  DEV1 EQU 0x1000

- Read/write code
  
  LDR r1, =DEV1 ; set up device address
  LDR ro, [r1] ; read DEV1
  MOV ro, #8 ; set up value to write
  STR ro, [r1] ; write value to device
Peek and Poke

- Traditional HLL interfaces:

```c
int peek (char *location)
{
    return *location;
}

int poke (char *location, char newval)
{
    (*location) = newval;
}
```
Busy-Wait Output

- Simplest way to program device
  - Use instructions to test when device is ready

```c
current_char = mystring;
while (*current_char != \0) {
  while (peek (OUT_STATUS) != 0);
  poke (OUT_CHAR, *current_char);
  current_char++;
}
```

The output status register’s value is 1 when the device is busy writing.
Interrupt I/O

- Busy-wait (or polling) is very inefficient
  - CPU can’t do other work while testing device
  - Hard to do simultaneous I/O

- Interrupts allow a device to change the flow of control in the CPU
  - Causes subroutine call to handle device
Interrupt Interface

- Interrupt request
- Interrupt acknowledgment
- Data/address

CPU

Interrupt Interface Diagram:
- CPU
- Status register
- Data register
- Mechanism
Interrupt Behavior

- Based on subroutine call mechanism
- Device asserts interrupt request
- CPU asserts interrupt acknowledge when it can handle the interrupt
- Interrupt forces next instruction to be a subroutine call to a predetermined location
- Return address is saved to resume executing foreground program
Priorities and Vectors

- Two mechanisms allow us to make interrupts more specific:
  - Priorities determine what interrupt gets CPU first
  - Vectors determine what code is called for each type of interrupt
- Mechanisms are orthogonal: most CPUs provide both
Prioritized Interrupts

- CPU
- device 1
- device 2
- device n
- L1 L2 .. Ln
- interrupt acknowledge
Interrupt Prioritization

▪ **Masking**
  • Interrupt with priority lower than current priority is not recognized until pending interrupt is complete

▪ **Non-maskable interrupt (NMI)**
  • Highest-priority, never masked
  • Often used for power-down
Example: Prioritized I/O

Prioritized I/O: interrupts

Prioritized I/O: foreground
Interrupt Vectors

- Allow different devices to be handled by different code
- Interrupt vector table:

<table>
<thead>
<tr>
<th>Interrupt vector table head</th>
<th>handler 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>handler 1</td>
</tr>
<tr>
<td></td>
<td>handler 2</td>
</tr>
<tr>
<td></td>
<td>handler 3</td>
</tr>
</tbody>
</table>
Interrupt Sequence

- CPU acknowledges request
- Device sends vector
- CPU calls handler
- Software processes request
- CPU restores state to foreground program
Interrupt Overhead

- Handler execution time
- Interrupt mechanism overhead
- Register save/restore
- Pipeline-related penalties
- Cache-related penalties
ARM Exceptions
Types of Exception

- Reset
- Undefined instruction
- Software interrupt (SWI)
- Prefetch abort
- Data abort
- IRQ (normal interrupt)
- FIQ (Fast interrupt)
## Processor Modes

- Mode changes by software control, or by external interrupts or exception processing

<table>
<thead>
<tr>
<th>Processor mode</th>
<th>Mode number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>User</td>
<td>usr</td>
<td>0b10000</td>
</tr>
<tr>
<td>FIQ</td>
<td>fiq</td>
<td>0b10001</td>
</tr>
<tr>
<td>IRQ</td>
<td>irq</td>
<td>0b10010</td>
</tr>
<tr>
<td>Supervisor</td>
<td>svc</td>
<td>0b10011</td>
</tr>
<tr>
<td>Abort</td>
<td>abt</td>
<td>0b10111</td>
</tr>
<tr>
<td>Undefined</td>
<td>und</td>
<td>0b11011</td>
</tr>
<tr>
<td>System</td>
<td>sys</td>
<td>0b11111</td>
</tr>
</tbody>
</table>
CPSR

M[4:0]: The mode bits
T: ARM(0), Thumb(1)
F: Enable(0) or disable(1) FIQ interrupts
I: Enable(0) or disable(1) IRQ interrupts
Exception Processing Modes

<table>
<thead>
<tr>
<th>Exception type</th>
<th>Mode</th>
<th>Normal address</th>
<th>High vector address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>Supervisor</td>
<td>0x00000000</td>
<td>0xFFFFF0000</td>
</tr>
<tr>
<td>Undefined instructions</td>
<td>Undefined</td>
<td>0x00000004</td>
<td>0xFFFFF0004</td>
</tr>
<tr>
<td>Software interrupt (SWI)</td>
<td>Supervisor</td>
<td>0x00000008</td>
<td>0xFFFFF0008</td>
</tr>
<tr>
<td>Prefetch Abort (instruction fetch memory abort)</td>
<td>Abort</td>
<td>0x0000000C</td>
<td>0xFFFFF000C</td>
</tr>
<tr>
<td>Data Abort (data access memory abort)</td>
<td>Abort</td>
<td>0x00000010</td>
<td>0xFFFFF0010</td>
</tr>
<tr>
<td>IRQ (interrupt)</td>
<td>IRQ</td>
<td>0x00000018</td>
<td>0xFFFFF0018</td>
</tr>
<tr>
<td>FIQ (fast interrupt)</td>
<td>FIQ</td>
<td>0x0000001C</td>
<td>0xFFFFF001C</td>
</tr>
</tbody>
</table>

Vector address 0x0000014/0xfffff0014 are reserved. The bit 13 of the System control coprocessor (CP15) register 1 selects the location of the exception vectors.
Co-processor

- Co-processor: added function unit that is called by instruction
  - Floating-point units are often structured as co-processors
- ARM allows up to 16 designer-selected co-processors
  - Floating-point co-processor uses units 1, 2
  - System control processor 15
## Exception Priorities

<table>
<thead>
<tr>
<th>Priority</th>
<th>Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Highest</td>
<td>Reset</td>
</tr>
<tr>
<td>2</td>
<td>Data Abort (including data TLB miss)</td>
</tr>
<tr>
<td>3</td>
<td>FIQ</td>
</tr>
<tr>
<td>4</td>
<td>IRQ</td>
</tr>
<tr>
<td>5</td>
<td>Imprecise Abort (external abort) - ARMv6</td>
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<tr>
<td>6</td>
<td>Prefetch Abort (including prefetch TLB miss)</td>
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<tr>
<td>Lowest</td>
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<tr>
<td></td>
<td>Undefined instruction</td>
</tr>
<tr>
<td></td>
<td>SWI</td>
</tr>
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</table>
## Register Organization

<table>
<thead>
<tr>
<th>User</th>
<th>System</th>
<th>Supervisor</th>
<th>Abort</th>
<th>Undefined</th>
<th>Interrupt</th>
<th>Fast interrupt</th>
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<tbody>
<tr>
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<tr>
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<td>SPSR_fiq</td>
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<td></td>
<td></td>
<td></td>
<td>SPSR_fiq</td>
</tr>
</tbody>
</table>
IRQ

▪ On entry

- $R14_{\text{irq}} = \text{address of next instruction to be executed} + 4$
- $\text{SPSR}_{\text{irq}} = \text{CPSR}$
- $\text{CPSR}[4:0] = 10010$ /* IRQ mode */
- $\text{CPSR}[5] = 0$ /* ARM state */
- $\text{CPSR}[7] = 1$ /* disable normal interrupts */
- $\text{PC} = 0x00000018$

▪ On exit (by programmer)

- $\text{SUBS PC, R14, #4}$ /* SPSR is moved to CPSR */
FIQ

**On entry**

- $R_{14\_fiq} = \text{address of next instruction to be executed} + 4$
- $SPSR\_fiq = \text{CPSR}$
- $\text{CPSR}[4:0] = 10001$ /* FIQ mode */
- $\text{CPSR}[5] = 0$ /* ARM state */
- $\text{CPSR}[6] = 1$ /* disable fast interrupts */
- $\text{CPSR}[7] = 1$ /* disable normal interrupts */
- $PC = 0x0000001C$

**On exit (by programmer)**

- $\text{SUBS PC, R}_{14}, \#4$ /* SPSR is moved to CPSR */
ARM Supervisor Mode

- Use SWI instruction to enter supervisor mode, similar to subroutine:
  - `SWI CODE_1`
- Sets PC to 0x08
- Arguments to SWI is passed to supervisor mode code
- Saves CPSR in SPSR
ARM Interrupt Latency

- **Worst-case latency to respond to interrupt is 27 cycles:**
  - Two cycles to synchronize external request
  - Up to 20 cycles to complete current instruction
  - Three cycles for data abort
  - Two cycles to enter interrupt handling state

- **Best-case latency is 4 cycles.**
Jasmine OpenSSD Code
Entry Point

- @ ./target_spw/init_rvds.s

```assembly
ENTRY

B reset_handler ; reset
B . ; undefined instruction
B . ; SWI
B . ; prefetch abort
B . ; data abort
NOP ; reserved vector
B irq_handler ; IRQ
B fiq_handler ; FIQ

reset_handler

; IRQ mode stack
MSR CPSR_c, #MODE_IRQ:OR:I_BIT:OR:F_BIT
LDR R13, =|Image$ER_IRQ_STACK$$ZI$$Limit|

; FIQ mode stack
MSR CPSR_c, #MODE_FIQ:OR:I_BIT:OR:F_BIT
LDR R13, =|Image$ER_FIQ_STACK$$ZI$$Limit|

; SYSTEM mode stack
; SYSTEM mode is the main mode of Barefoot firmware.
MSR CPSR_c, #MODE_SYS:OR:I_BIT:OR:F_BIT
LDR R13, =|Image$ER_SYS_STACK$$ZI$$Limit|

BL init_jasmine
BL Main
B . ; should not reach here
```
Disabling/Enabling Interrupts

- @ ./target_spw/init_rvds.s)

```assembly
disable_interrupt
  MRS R0, CPSR
  ORR R0, R0, #0xC0
  MSR CPSR_c, R0
  BX LR

enable_interrupt
  MRS R0, CPSR
  BIC R0, R0, #0xC0
  MSR CPSR_c, R0
  BX LR
```