Flash Translation Layers I

Jin-Soo Kim (jinsookim@skku.edu)
Computer Systems Laboratory
Sungkyunkwan University
http://csl.skku.edu
NAND Constraints
No In-Place Update

- Can’t overwrite data
- Previous data should be erased
- The erase unit is much larger than the read/write unit
  - Read/write unit: page (4KB, 8KB)
  - Erase unit: block (64 ~ 128 pages)
Bit Errors

- Error correction codes (ECC) in spare area
- Hardware vs. software

<table>
<thead>
<tr>
<th>Error Correction Level</th>
<th>Bits Required in the NAND Flash Spare Area</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hamming</td>
</tr>
<tr>
<td>1</td>
<td>13</td>
</tr>
<tr>
<td>2</td>
<td>N/A</td>
</tr>
<tr>
<td>3</td>
<td>N/A</td>
</tr>
<tr>
<td>4</td>
<td>N/A</td>
</tr>
<tr>
<td>5</td>
<td>N/A</td>
</tr>
<tr>
<td>6</td>
<td>N/A</td>
</tr>
<tr>
<td>7</td>
<td>N/A</td>
</tr>
<tr>
<td>8</td>
<td>N/A</td>
</tr>
<tr>
<td>9</td>
<td>N/A</td>
</tr>
<tr>
<td>10</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Source: Micron Technology, Inc.
Bad Blocks

- Factory-marked bad blocks
- Run-time bad blocks

- Bad block table
- Bad block remapping
Limited Lifetime

- Limited program/erase cycles
- 100K for SLCs
- 3K ~ 10K for MLCs
- Wear-leveling
Page Programming

- **NOP**
  - The number of partial-page programming is limited
  - 1 / sector for most SLCs (4 for 2KB page)
  - 1 / page for most MLCs

- **Sequential page programming**
  - Pages should be programmed sequentially inside a block
  - For large block SLCs and MLCs
Paired Pages in MLCs

- Performance difference
- Interference

![Diagram showing Vth and page values for I/O-split and page-swap MLCs]

<table>
<thead>
<tr>
<th>Page</th>
<th>LSB Page</th>
<th>MSB Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Page i</td>
<td>11 10 01 00</td>
<td>1 0 0 1 0 0 1 1</td>
</tr>
<tr>
<td>Page j</td>
<td>11 10 01 00</td>
<td>1 1 0 0 1 1 0 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Beauty and the Beast

- **NAND Flash memory is a beauty**
  - Small, light-weight, robust, low-cost, low-power non-volatile device

- **NAND Flash memory is a beast**
  - Much slower program/erase operations
  - No in-place-update
  - Erase unit > write unit
  - Limited lifetime (3K ~ 100K P/E cycles)
  - Bad blocks, ...
Introduction to Flash Translation Layers
Storage Abstraction

- Abstraction given by block device drivers:

- Operations
  - Identify(): returns N
  - Read (start sector #, # of sectors)
  - Write (start sector #, # of sectors, data)

Source: Sang Lyul Min (Seoul National Univ.)
What is FTL?

- A software layer to make NAND flash fully emulate traditional block devices (or disks)

Source: Zeen Info. Tech.
Flash Cards Internals
SSD Internals

INDILINX
Barefoot Controller 175 MHz

SRAM (96KB)
Controller

ROM
Controller

ARM7TDMI-S
Core

Clock
Generator

APB Bridge

System Bus

NAND Controller

Buffer Manager

SATA Device

DRAM Controller

Memory Utility

 UART

GPIO

Timer

WDC

PMU

ICU

JTAG

DRAM Access Bus

NAND Flash

SATA Host interface

DRAM

JTAG debug port
Implementing FTLs

Flash Cards, SSDs

Applications
Operating System
File Systems
Block Device Driver
Flash Translation Layer
NAND Controller
NAND Flash Memory

Embedded Flash Storage

Applications
Operating System
File Systems
Block Device Driver
Flash Translation Layer
NAND Controller
NAND Flash Memory
For Performance

- Indirect mapping (address translation)
- Garbage collection
- Over-provisioning
- Hot/cold data identification/separation
- Interleaving over multiple channels/flash chips/planes
- Request scheduling
- Buffer management, ...
For Reliability

- Bad block management
- Wear-leveling
- Power-off recovery
- Error correction code (ECC)
- ...
Other Features

- Encryption
- Compression
- Deduplication
- ...
Basic Mapping Techniques
Naïve Block Mapping

- Each table entry maps one block
- Small RAM usage
- Inefficient handling of small writes
Example (1)

- $W = \langle\{4,5,6,7\}, \{1\}\rangle$
  - write ($\{4,5,6,7\}$, ABCD)
Example (2)

- \( W = \langle \{4, 5, 6, 7\}, \{1\} \rangle \)
  - write (\( \{4, 5, 6, 7\}, \text{ABCD} \))
  - write (\( \{1\}, \text{E} \))
ANAND Scheme

- M-Systems
- US Patent 5,937,425
- Uses one or more replacement blocks
- Data is written to an unwritten physical page with the desired physical page offset

\[ W = \langle\{1\}, \{4,5\}, \{8\}, \{10\}, \{8\}\rangle \]
Naïve Page Mapping

- Most flexible
- Efficient handling of small writes
- Large memory footprint
  - 32MB for 32GB MLC (4KB page)
- Sensitive to the amount of reserved blocks
- Performance affected as the system ages
Example (1)

- $W = \langle\{1\}, \{2\}, \{8\}, \{1\}, \{2\}, \{12,13\}, \{9\}\rangle$
  - write ($\{1\}$, A)
Example (2)

- $W = \langle \{1\}, \{2\}, \{8\}, \{1\}, \{2\}, \{12,13\}, \{9\} \rangle$

  - write ($\{1\}, A$)
  - write ($\{2\}, B$)
Example (3)

- $W = \langle \{1\}, \{2\}, \{8\}, \{1\}, \{2\}, \{12,13\}, \{9\} \rangle$
  - write ($\{1\}, A$)
  - write ($\{2\}, B$)
  - write ($\{8\}, C$)
Example (4)

- $W = <\{1\}, \{2\}, \{8\}, \{1\}, \{2\}, \{12,13\}, \{9\}>
  - write ($\{1\}$, A)
  - write ($\{2\}$, B)
  - write ($\{8\}$, C)
  - write ($\{1\}$, D)
Example (5)

- \( W = \langle \{1\}, \{2\}, \{8\}, \{1\}, \{2\}, \{12,13\}, \{9\} \rangle \)
  - write (\{1\}, A)
  - write (\{2\}, B)
  - write (\{8\}, C)
  - write (\{1\}, D)
  - write (\{2\}, E)
Example (6)

- $W = \langle \{1\}, \{2\}, \{8\}, \{1\}, \{2\}, \{12,13\}, \{9\} \rangle$
  
  - write ($\{1\}$, A)
  - write ($\{2\}$, B)
  - write ($\{8\}$, C)
  - write ($\{1\}$, D)
  - write ($\{2\}$, E)
  - write ($\{12,13\}$, FG)
Example (7)

- $W = \langle \{1\}, \{2\}, \{8\}, \{1\}, \{2\}, \{12,13\}, \{9\}\rangle$
  - write (\{1\}, A)
  - write (\{2\}, B)
  - write (\{8\}, C)
  - write (\{1\}, D)
  - write (\{2\}, E)
  - write (\{12,13\}, FG)
  - write (\{9\}, H)
Victim Selection Policies

- **Greedy**
  - A block with the largest amount of invalid data

- **Cost-benefit [Kawaguchi 1995]**
  - A block with the maximum \( \frac{\text{benefit}}{\text{cost}} = \frac{(1 - u)}{2u} \times \text{age} \)
  - \( u \): utilization
  - \( \text{age} \): the time since the most recent modification

- **Cost Age Times (CAT) [Chiang 1999]**
  - A block with the minimum \( \frac{u}{(1 - u) \times \text{age}} \times \text{count} \)
  - \( \text{count} \): erase count