Makefile

- **Simplify compiling source codes**
  - Which do you want?

```
$ g++ -o test main.cpp test.cpp hello.cpp
$ rm main.o test.o hello.o
```

VS.

```
$ make
$ make clean
```

Macro

- **Similar to variable**

```
# Makefile
COMPILER= g++
WARNING= -W3
LIBS = -lncurses
…
```

- **Internal macro**
  - $@ : Name of the file to be made
  - $? : Names of the changed dependents
  - $^ : List of dependents

Macro Example

```
# Makefile
CC= g++
CFLAGS= -W2
TARGET= hello
$(TARGET): main.o hello.o
	$(CC) $(CFLAGS) -o $(TARGET) main.o hello.o
main.o: main.cpp
	$(CC) $(CFLAGS) -c main.cpp
hello.o: hello.cpp
	$(CC) $(CFLGAS) -c hello.cpp
clean:
	rm *.o hello
```

CXX

```
OBJECT= main.o hello.o
all: $(TARGET)
$(TARGET): $(OBJECTS)
	$(CC) $(CFLAGS) -o $@ $^
```

Dependency

- **Target “hello” is dependent on main.o & hello.o**

```
# Makefile
CC= g++
CFLAGS= -W2
TARGET= hello
$(TARGET): main.o hello.o
	$(CC) $(CFLAGS) -o main.o hello.o
main.o: main.cpp
	$(CC) $(CFLAGS) -c main.cpp
hello.o: hello.cpp
	$(CC) $(CFLGAS) -c hello.cpp
clean:
	rm *.o hello
```

Etc

- **Suffix**

```
#Makefile
.c.o:
        $(CC) $(CFLAGS) -o $@ $^
```

.SUFFIXES: .c .o

- **Macro subsitution**

```
MY_VAR= aa bb
MY_VAR2= $(MY_VAR:bb=cc)
OBJS= main.o hello.o
SRCS= $(OBJS:.o=.cpp)
```